THAT WHICH IS CLAIMED IS:

1. A microprocessor comprising a central processing unit (2) having an arithmetic and logic unit (3) with at least two inputs and one input which is fed-back to one of said inputs through data paths, the arithmetic and logic unit (3) including means for performing arithmetic and logic operations on the binary words temporarily stored within registers (5) in the central processing unit (2), the central processing unit further comprising a shift unit (4) interposed in the data path of the arithmetic and logic unit (3), and comprising means for performing shift operations on the bits of the binary words that are supplied thereto, and selection means for selecting a shift operation to be performed,

characterized in that it further comprises inverting means (4, 4') for inverting the ordering of bits of binary words that applied thereto, which means are interposed in the data path of the arithmetic unit, and selection means for selecting the inversion operation when the latter is required.

2. The microprocessor according to claim 1, characterized in that the inverting means (4) are integrated within the shift unit (4).

3. The microprocessor according to claim 2, characterized in that the shift unit (4) is arranged upstream one of the inputs of the arithmetic and logic unit (3).

4. The microprocessor according to claim 2, characterized in that the shift unit (4) is arranged at the output of the arithmetic and logic unit (3).

5. The microprocessor according to any of claims 1 to 4, characterized in that the shift unit comprises as many demultiplexers (21 to 24) as there are bits in the words to be processed (30), each demultiplexer having a binary input and as many binary outputs as there are shift operations to be performed, the outputs of the demultiplexers each being connected to one line of a bus (25) connected to the output (20) of the shift unit and having at least as many lines as there are bits in the words to be processed, the demultiplexers (21 to 24) receiving as an input one respective bit of the word applied as an input (19) to the shift unit (4), and outputting the value of the bit input at one of the demultiplexer's outputs, which is selected as a function of the shift operation to be performed, the line of the bus (25) to which each output of each demultiplexer is connected being chosen in accordance with the rank, within the word to be processed, of the bit input to the demultiplexer and with the shift operation corresponding to the demultiplexer output.

6. The microprocessor according to any of claims 1 to 5, characterized in that the inverting means (4') for inverting the ordering of bits in binary words are arranged upstream the shift unit (4).